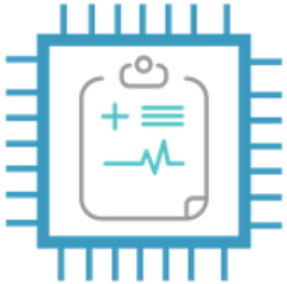

York TOHOKU KAISERSLAUTERN LEEDS Manchester spintec symposium

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Overview of Magnetic Devices at Imec

Sebastien Couet, Thanks to the whole MRAM team!

Introduction of IMEC

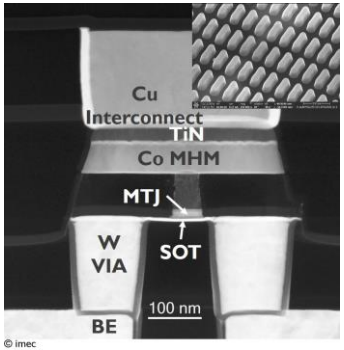
imec

@ Leuven

300 mm wafer

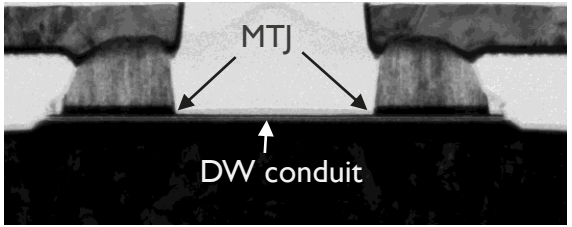
IMEC: R&D company, bridge the gap between fundamental research and industry in nanoelectronic
~ 5,000 researchers, 900 PhD students, 800 industrial resident from > 90 nationalities, 12,000 m^2 cleanroom

SPINTRONICS at IMEC



Memory application:
- STT-MRAM
- SOT-MRAM
- VCMA-MRAM

Logic application:
- Spin wave
- Magnetoelectrics
- DW-based



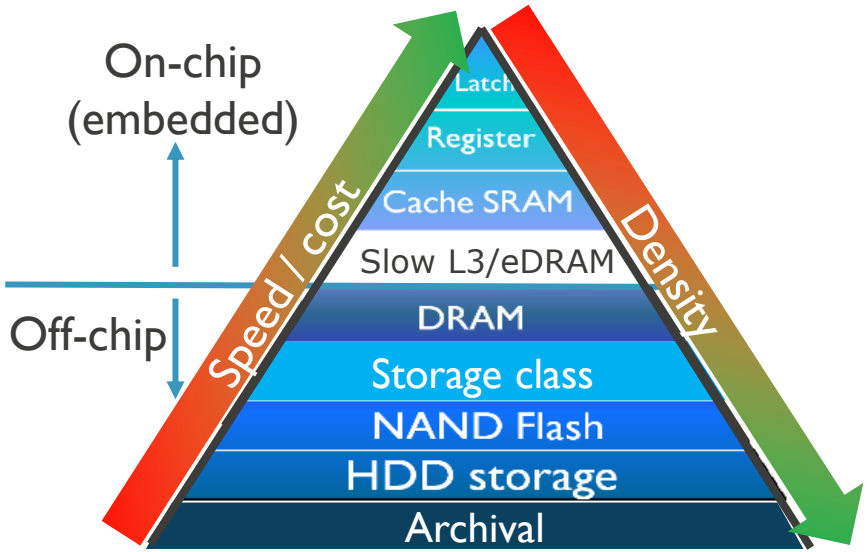
Acknowledgment to Imec magnetic team!

- **Thin Films** S. Mertens, R. Carpenter, G. Talmelli, X. Piao, W. Janssens, M. Ben Chroud, M. Wisjshoff
- **Etch** N. Franchina Vergel, R. Blanc, H. Puliyalil, Y. Canvel , L. Souriau
- **Litho** M. Pak, P. Rincon Delgadillo
- **CMP** D. Tsvetanova, B. Kenens, K. Devriendt
- **Integration** N. Jossart, S. Houshmand Sharifi, G. Potoms, A. Trovato, F. Yasin, L. Angelo Labatte, A. Palomino Lopez
- **MRAM Device** S. Rao, W. Kim, K. Cai, M. Gama, V. D. Nguyen, A. Kumar, P. Hendricks, V. Kateel, K. Fan, T. Ravsher, A. Fantini, D. Favoro, D. Giuliano, S. Ranjbar
- **Spin logic device** F. Ciubotaru, C. Adelmann, F. Meng, Anais Guerenneur, Daniele Narducci, F. Luciano, E. Van Meirvenne
- **Reliability** S. Van Beek
- **Physical Charac.** O. Richard, U. Celano J. Patil
- **Modeling** K. Sankaran, N. Ao, G. Pourtois
- **Management** A. Furnémont, G.S. Kar, L. Goux, L. Di Piazza, D. Crotti, I. Asselberghs, K. Wostyn
- **Collaborations** P. Gambardella, V. Krizakova, M. Hoffman ETH Zürich
  S. Hamidoui TU Delft
  K. Garello, L. Vila spintec

Outline

- Why magnetic memories?
- MRAM for cache-level applications: what do we need?
- Device concepts and status
- MTJ technology challenges
  - TMR
  - Stochastics
  - Write: STT, SOT, VCMA
  - Next gen transducers?
- Take-away

The memory pyramid



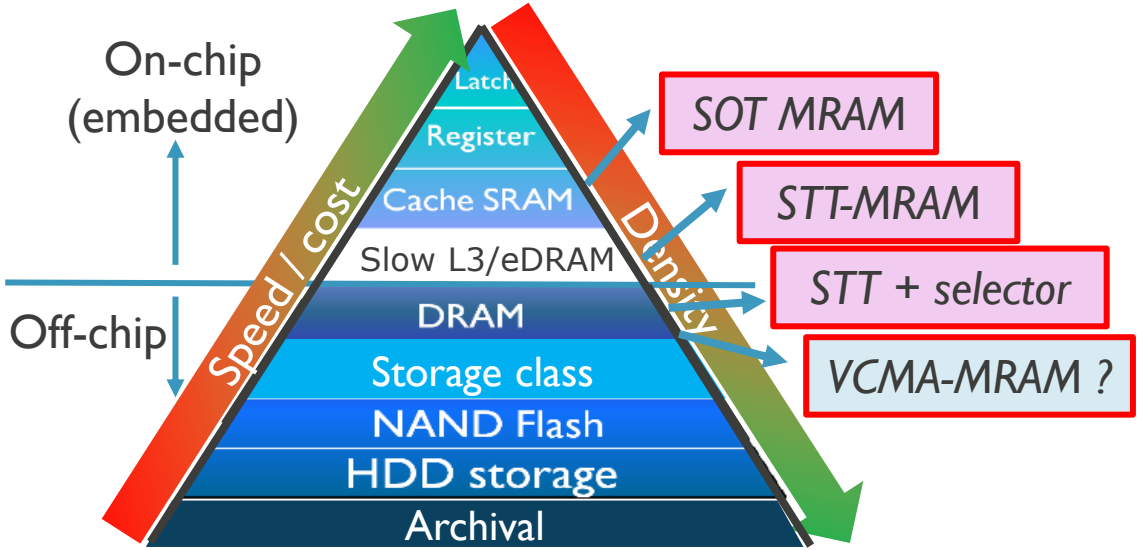
Since last 40 years...

(Mostly) 3 types of memories:

SRAM	Fast on-chip
DRAM	Fast off-chip
NAND	Non-volatile storage

- Highly optimized
- Fully adopted
- **SRAM:**
  - ✓ Ghz speed, low power, tunable, 'free' process
  - × Big cell size = Mb capacity, marginal scaling
  - × Standby leakage

The memory pyramid



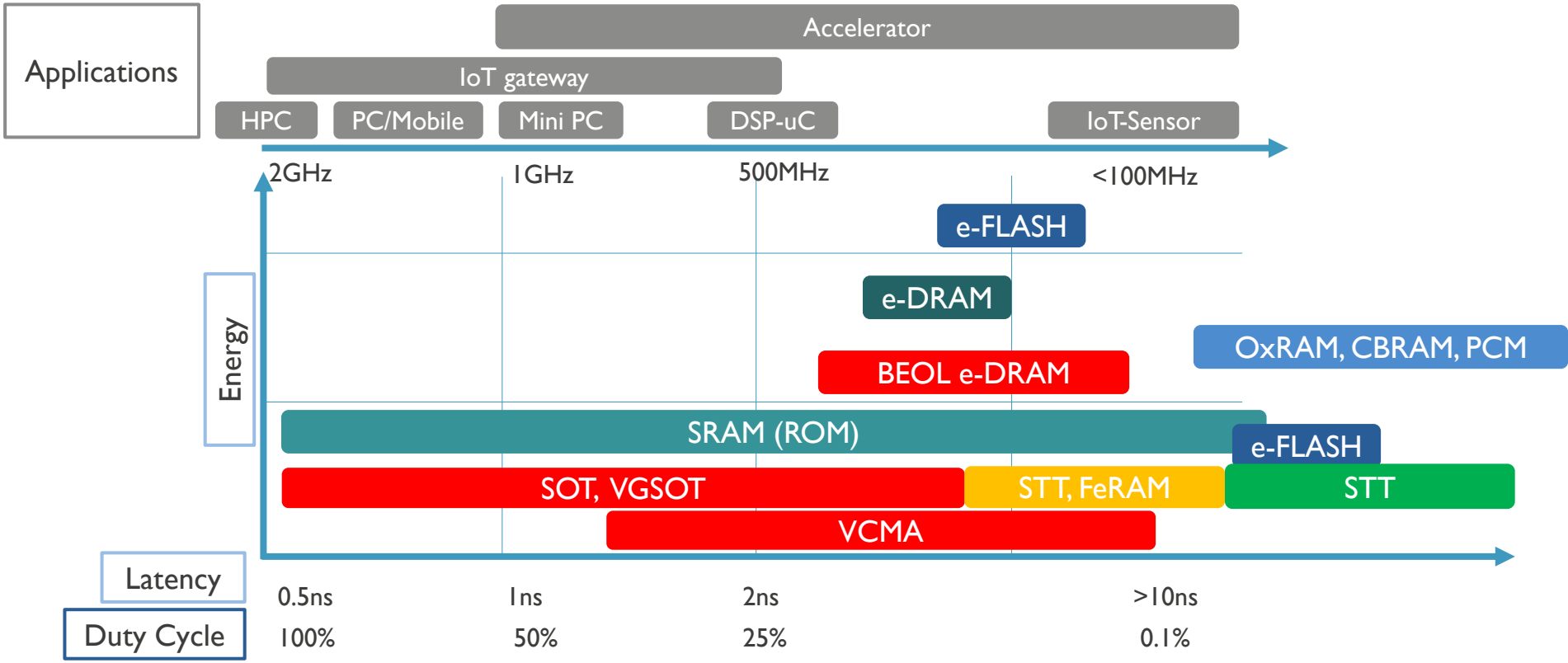
Fundamental figure of merit: **PPAC**
Power – **P**erformance – **A**rea - **C**ost

Key features of MRAMs

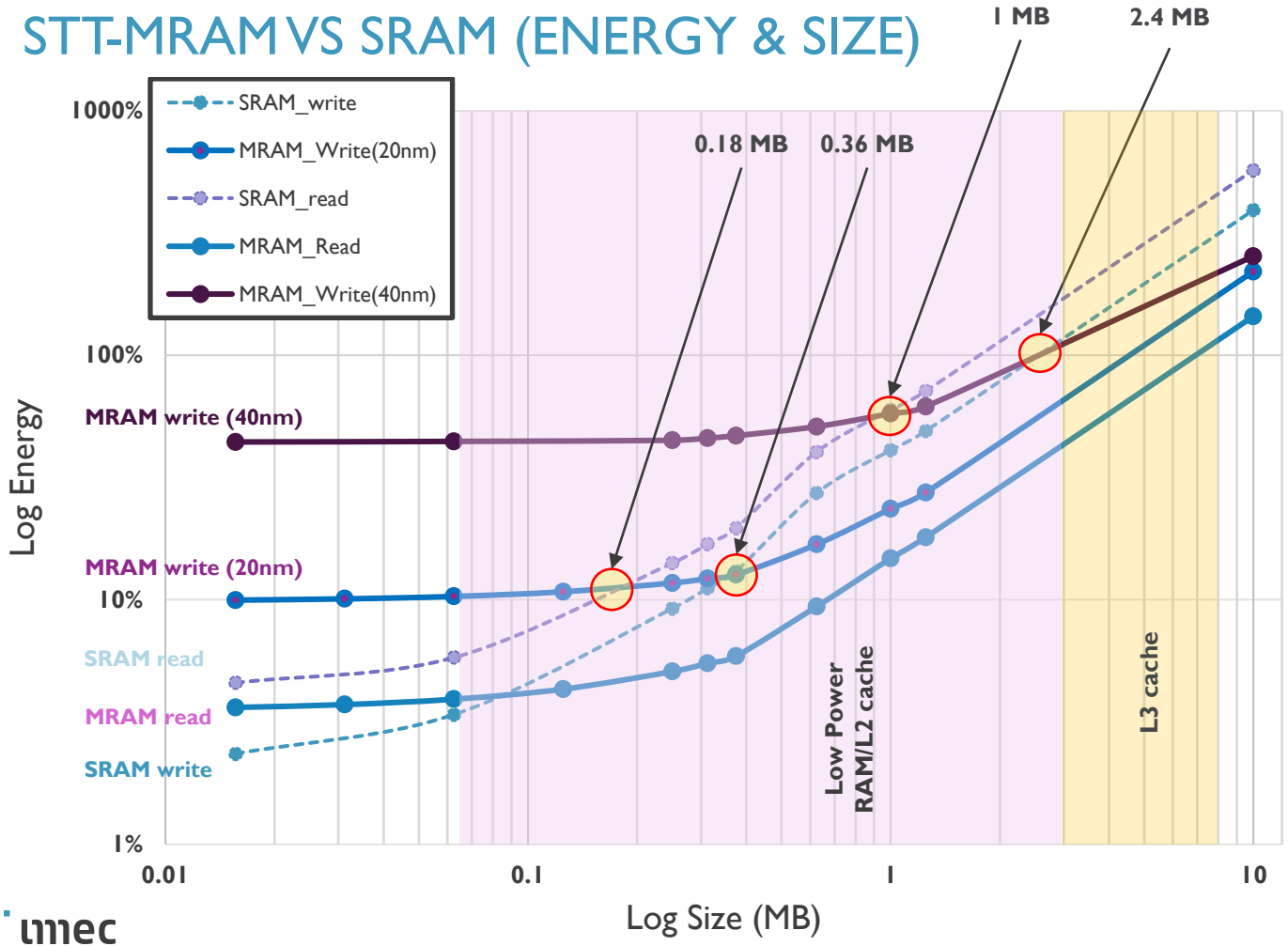
- 0.3 to 100ns speed
- Non-volatile
- Good endurance
- CMOS compatible V_{sw}

- High current
- Low MR window

Embedded memory applications space: Future



STT-MRAM VS SRAM (ENERGY & SIZE)

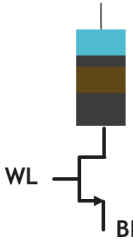
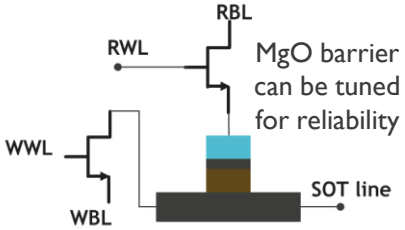
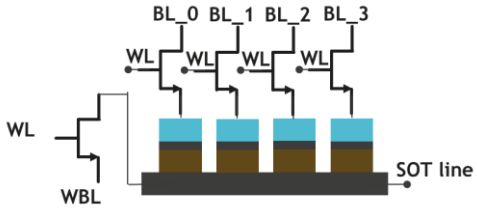
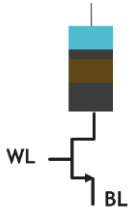


- STT-MRAM density gain limited by FEOL drive transistor
- Cross-over SRAM/MRAM in terms of read/write energy once array reach few megabytes

S. Sakhare et al., IEDM 2018

imec

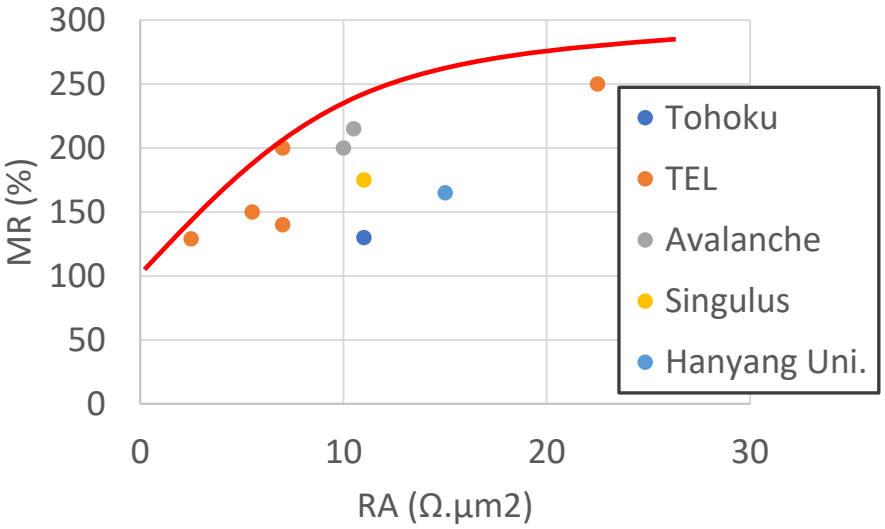
Magnetic Memory (e-NVM) Options For Cache Replacement

	SPIN TRANSFER TORQUE (STT)	SPIN ORBIT TORQUE (SOT)	VOLTAGE GATED SPIN ORBIT TORQUE (VGSOT)	VOLTAGE CONTROL MAGNETIC ANISOTROPY (VCMA)
	 MTJ optimized for **current-based** operation, low R	 MgO barrier can be tuned for reliability	 Single transistor in write path, cell selectivity through voltage gate	 MTJ optimized for **voltage-based** operation, higher R
Performance	OK for last level cache	OK for all levels cache. GHz capability	OK for all level cache. GHz capability	To be defined
Cost, area	~50% gain over HD SRAM	Similar to HD SRAM	>60% gain over HD SRAM	~50% gain over HD SRAM
Power	Big gain at system level with use of non-volatility	Gain over HP SRAM	Big gain over HP/HD SRAM	Voltage controlled, lowest power
Reliability	Difficult for high endurance specs (failing tail bits)	Good. Read and write paths separated	Good. Read and write paths separated	Probably OK (low current device)
Maturity	Ready	Research	Research	Exploratory

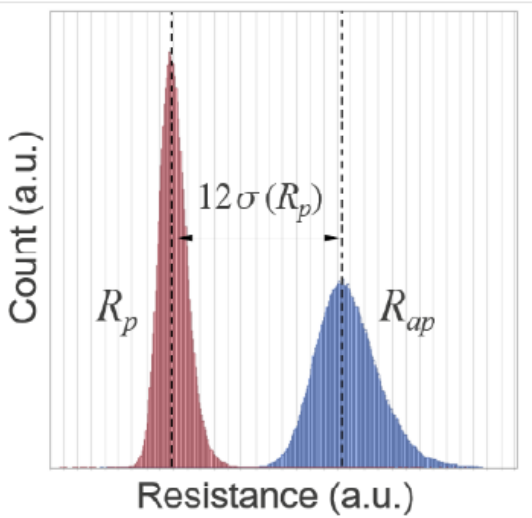
MTJ technology challenges

TMR read

Speed/density bottleneck



Published blanket TMR/RA of p-MTJ from key groups



Higher TMR required for bigger arrays

TMR read-out is a limitation of MTJ technology

- Up to 300% (x4)
- Low compared to other memory device (10-1000...)

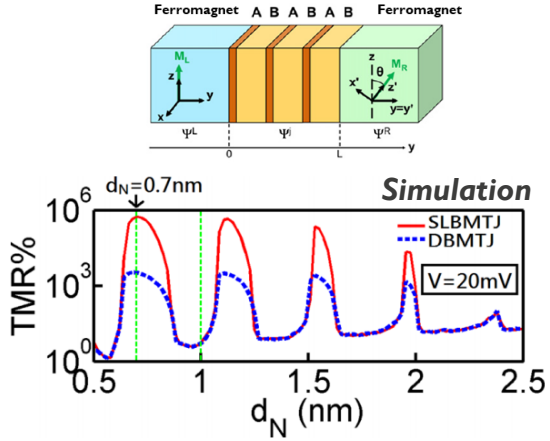
- Lead to slow read times (5-10ns), bigger circuitry
- Put more challenges on fabrication uniformity
  - Pillar diameter
  - MgO inhomogeneity
  - ...

High TMR attempt

Superlattice barrier

Goal:
Creation of quantum well between oxide to strongly enhance TMR

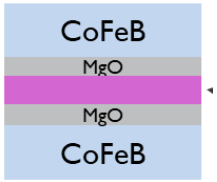
Concept:
Insulator/ metal or insulator/magnet superlattice



Can we make it?

[1] C. H. Chen et al., Appl. Phys. Lett. 104, 042405 (2014) http://dx.doi.org/10.1063/1.4863221

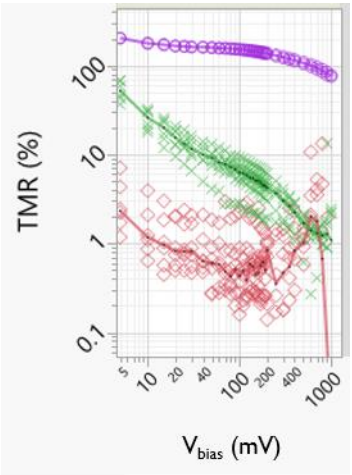
Evaluation by PVD @Imec – MgO/Spacer/MgO



Metal **A**, **B**, **C**
~0.5 to ~1.5nm thick

✓ Some metal provide OK TMR
× No oscillatory TMR

Likely require epi-like quality for quantum well formation

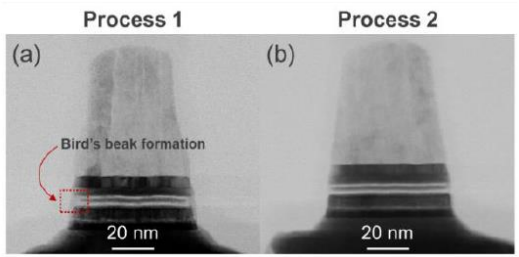


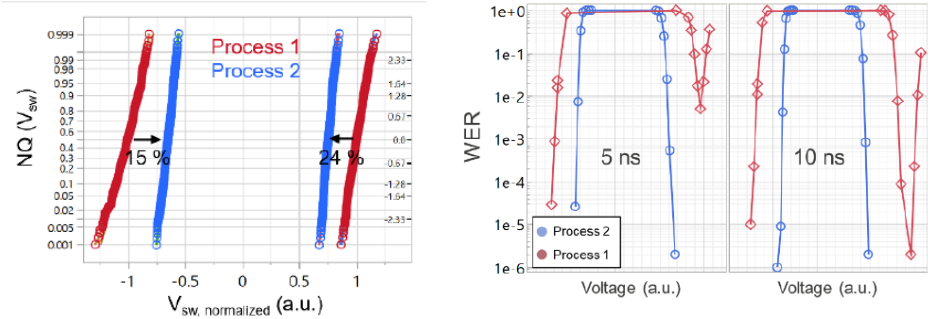
Fundamental research on **alternative read signal** or **TMR breakthrough** is (one of) of the key to the future of spintronics

Stochastic

Reliability/circuit overhead

Distributions and WER improvement by etch-optimization





S. Rao et al., IMW 2021 (imec)

Distributions

- Exists for all devices, ~ OK for MRAM
- **Impact:**
  - TMR = density limiter
  - Cell current need to be increase to include tailbits

WER/stochastics

- SRAM < 10^{-10}
- **Impact:**
  - Cell current need to increase (again) to achieve low error
  - Extra ECC creates speed and area overhead

This is impacting all devices: STT, SOT, VCMA, DW
How to drastically reduce stochastics?
Are there other engineering solution?
What new concept/physics could be envisioned?

STT efficiency challenge

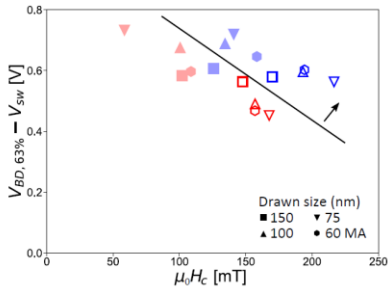
High speed switching (<= 5ns)

Sun's model*: $I > Ic_0$

$$\frac{1}{\langle \tau \rangle} = \left[\frac{2}{C + \ln\left(\frac{\pi^2 \xi}{4}\right)} \right] \frac{\mu_B P_{ref}}{e M_s V (1 + P_{ref} P_{free})} (I_{write} - I_{c0}) \quad (2)$$

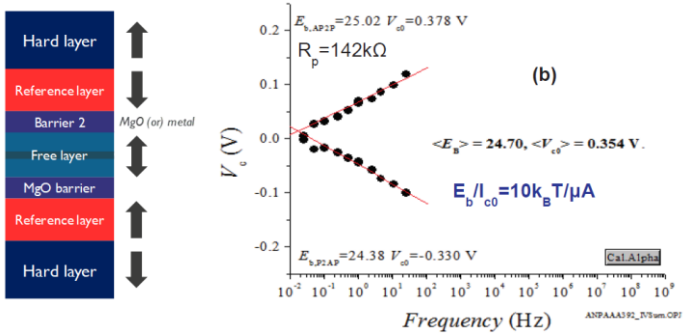
current reduction possible by
RL/FL ***polarization increase***
FL ***moment*** decrease

Material related



Switching reduction needed to improve breakdown margin at high Δ

Other alternative: extra torque via double MTJ



G. Hu et al., IEDM 2015

- TMR vs Isw trade-off
- More on this in Siddharth Rao's presentation, this symposium

Overall, challenging to make STT cache spec.

Main challenges:

- Reducing Vsw to Vbd margin at high speed
- WER is OK in best case but not amazing
- In general, limited material or engineering options

S. Van Beek et al., IRPS 978-1 (2021)

SOT-MRAM

Key features:

3-terminal device

- Write: Spin current
- Read: TMR readout

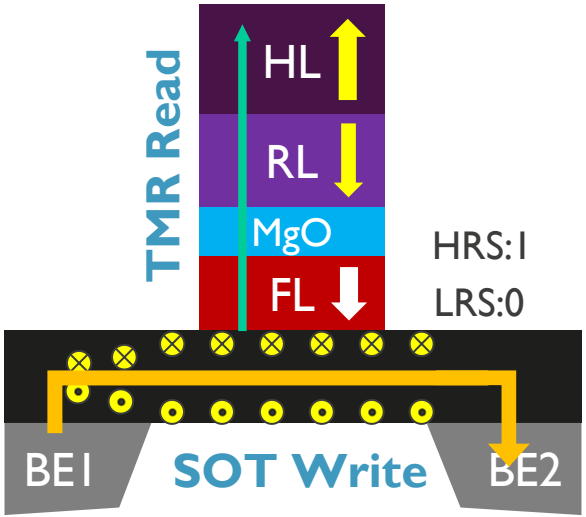
Separated paths for read & write

- Better endurance (>10^{14}) than STT

Faster switching than STT-MRAM

- **Sub-nanosecond** switching*

BEOL compatible**



Challenges:

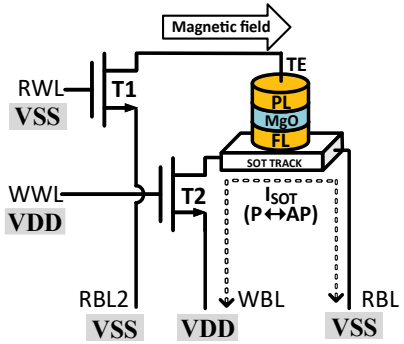
- Density (two transistors/bit), comparable to SRAM cell size***
- High switching current
- Field-free switching: magnetic hard mask****

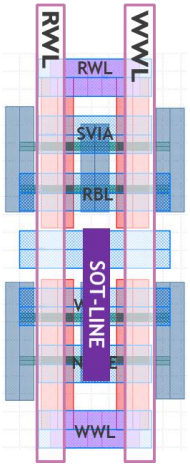
*K. Garello et al., VLSI, 81-82 (2018)
** S. Couet et al., VLSI (2021)
***M. Gupta et al., IEDM, 24.5. 1-24.5. 4 (2020)
****K. Garello et al., VLSI Circuit, T194-T195 (2019)

SOT-MRAM

Scaling challenge

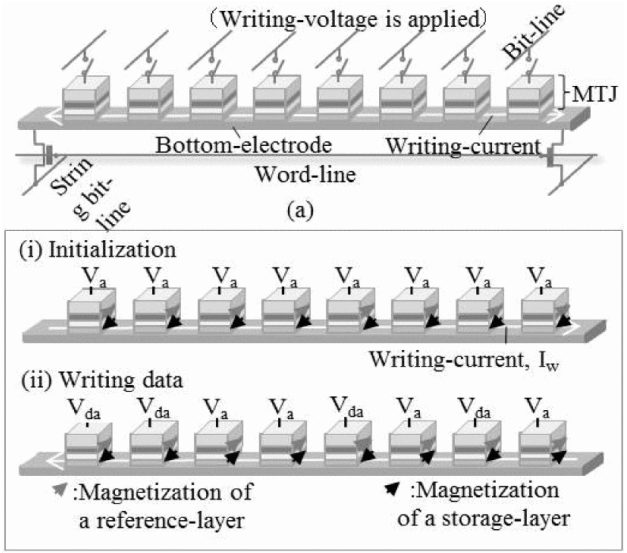
3-terminal is not helping!





Alternative
Reduce # of
terminal

H.Yoda et. al, IEDM (2016), VoCSM

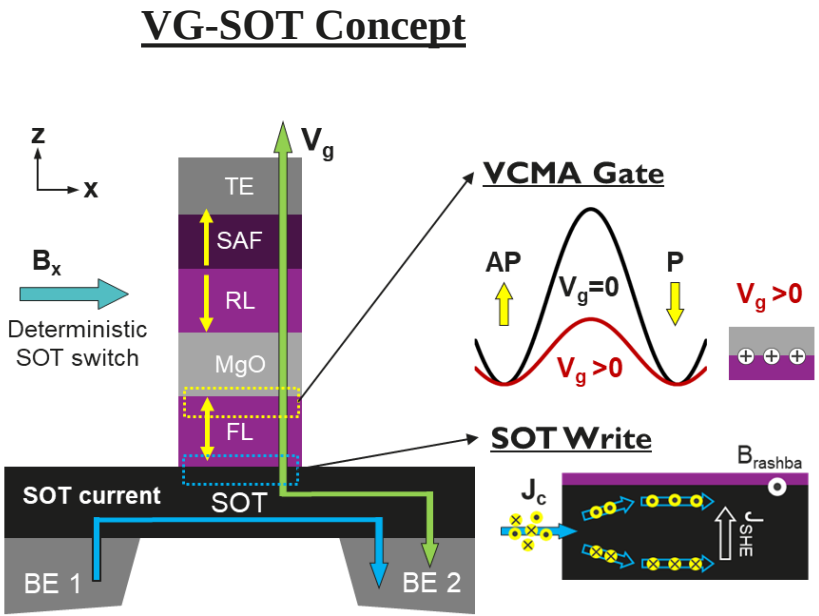


SOT simplest bit-cell design is 5 terminals
→ ~equals SRAM density (shared terminals)

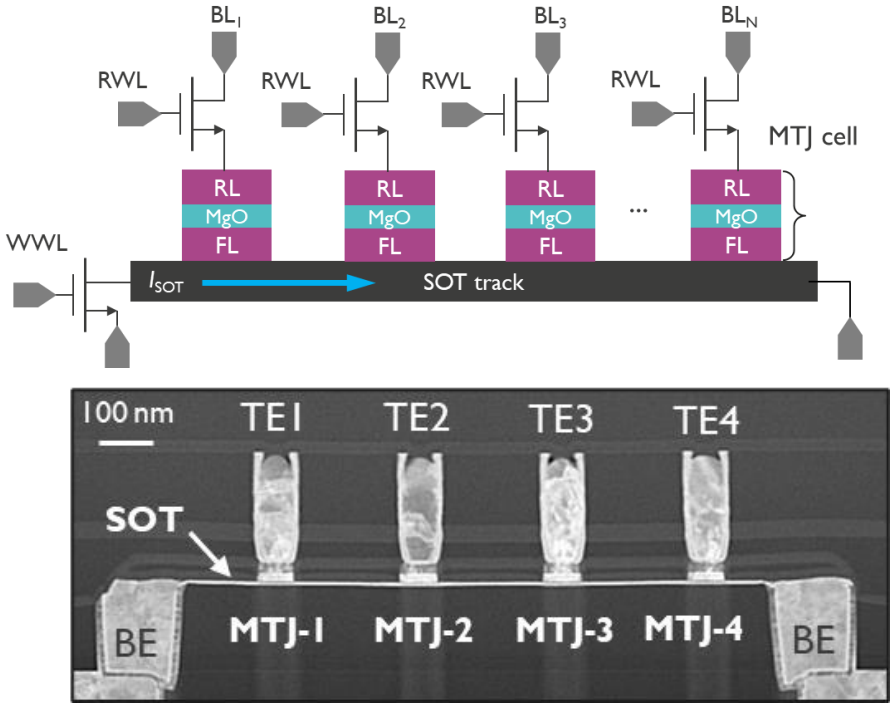
VCMA enables to **selectively write** many bits with a single SOT track

See Imec's work on this by K. Fan, this symposium

Voltage gated SOT device



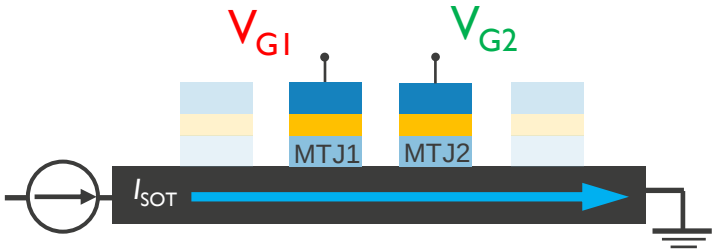
Multi-pillar schematic & integration

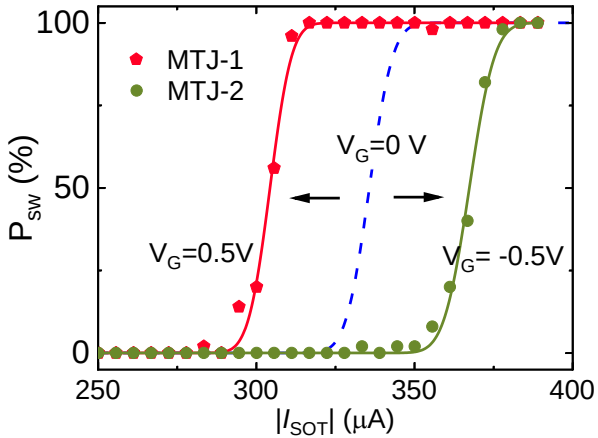


2T1R ⇒ **(n+2)TnR**

Selectivity demonstration - WER

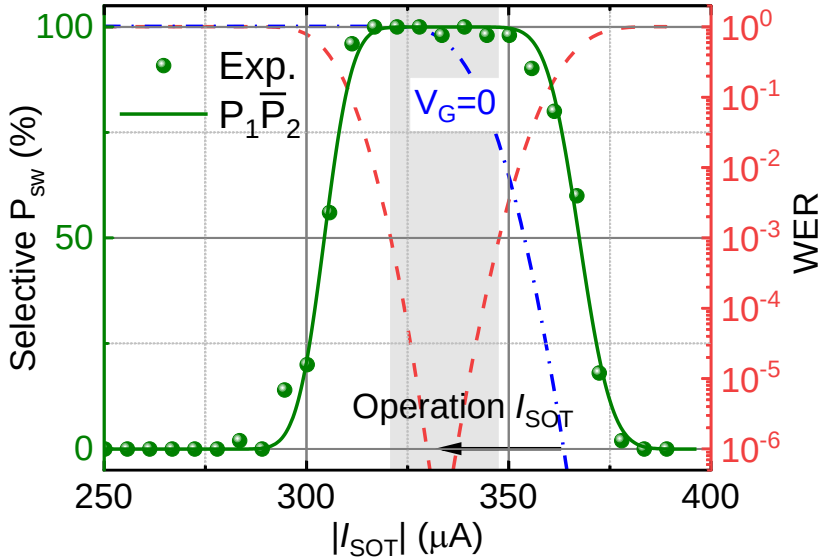
K. Cai et. al., 2022 VLSI





Statistic measurements:

- Individual P_{sw} of two bits

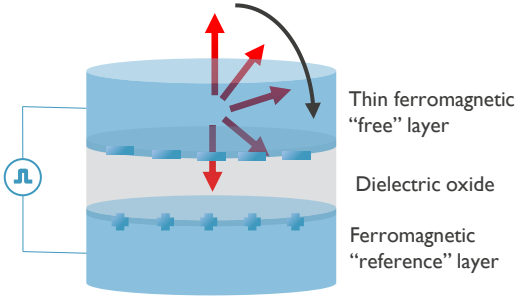


Joint P_{sw} of two bits ($P_1\overline{P_2}$):

- Working window
- low switching current

VCMA

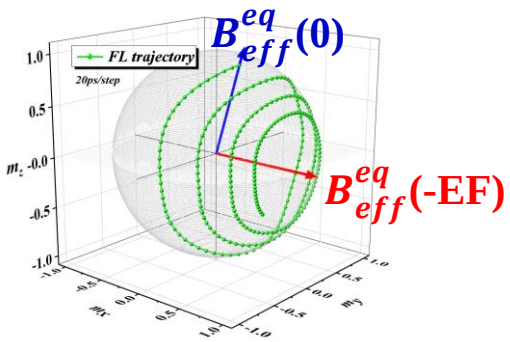
Voltage driven!

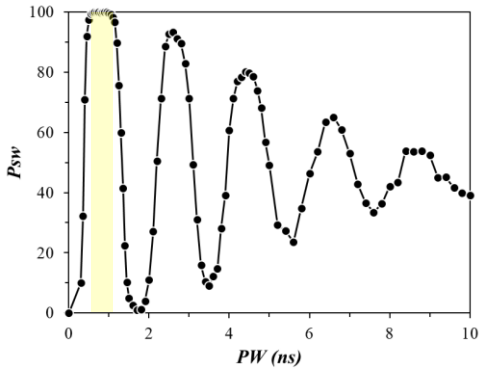


Voltage controlled device
(instead of current controlled)

Change in FL anisotropy energy by application of a voltage across magnet/dielectric interface

Precessional switching by dynamic re-orientation once perpendicular anisotropy ~ 0 under applied voltage and in-plane field





- **2-terminal**
  - Compact
- **High RA**
  - Voltage driven switching

VCMA = the dream device for speed, density and energy

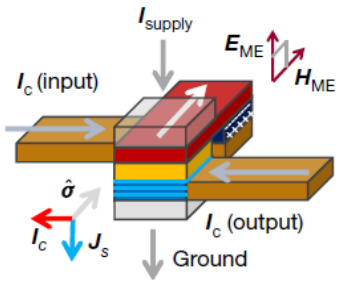
... BUT...

- Required VCMA coefficient looks challenging
  - See Robert Carpenter's presentation
- Timing circuit! Is it feasible at all?
  - How to deal with variability?
  - How to reach low WER?

Alternative transducers?

Voltage driven (for logic and/or memory)

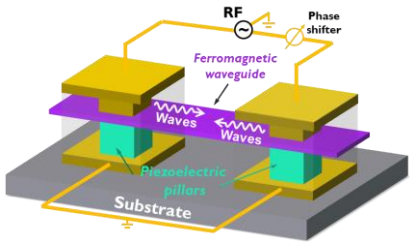
The only way forward?



MESO Logic (Intel)

Write: magneto-electric coupling of (multi)ferroelectric/ferromagnet
Read: inverse spin orbit torque

Excellent energetics
Unclear if ~100mV read signal can be generated

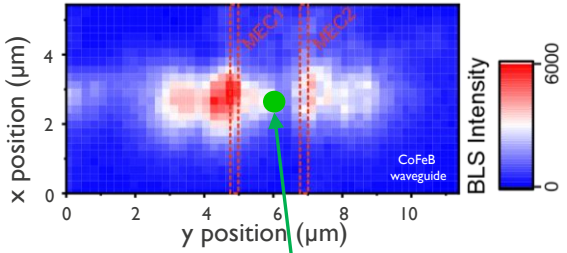


ME pillar for spinwave excitation (Imec)

- Very low power
- Wave computing
  - Quite disruptive for compute
- No retention = only for logic

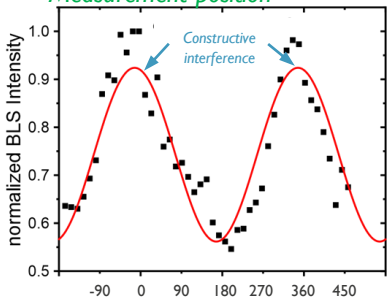
Interference of acoustic waves (phonons) generated by 2 ME pillars

2D BLS scan



$\Delta\varphi$ =180° phase difference ME_1 vs ME_2

Measurement position



Relative phase difference $\Delta\varphi$ between ME pillars (°)

Take-away

- Magnetic RAMs are one of the few emerging options to have a shot at SRAM replacement
  - Compared to alternatives, MRAM is most mature
- Key bottlenecks to tackle from fundamental perspective
  - **TMR is low** – TMR breakthrough or other read mechanism (voltage based?)
  - **Stochastics are not helping** – aside from engineering, can fundamental physics/new idea change the status quo?
  - **STT & SOT are getting there** - Will it be enough? Work on better switching efficiencies by material research & design is key
  - **VCMA seems like holy grail** – but precessional switching looks very hard

There are plenty of fundamental physics, material topics to be harnessed by scientific community, to unlock even more potentials for our field in micro-electronics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